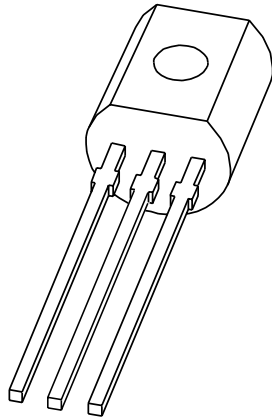


DATA SHEET



2N3904 NPN switching transistor

Product specification
Supersedes data of 1997 Jul 15

1999 Apr 23

NPN switching transistor

2N3904

FEATURES

- Low current (max. 200 mA)
- Low voltage (max. 40 V).

APPLICATIONS

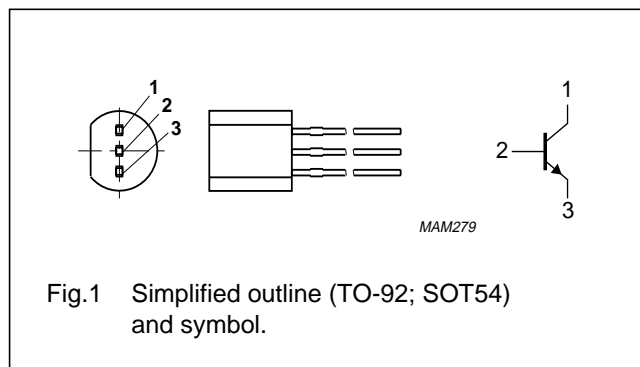
- High-speed switching.

DESCRIPTION

NPN switching transistor in a TO-92; SOT54 plastic package. PNP complement: 2N3906.

PINNING

PIN	DESCRIPTION
1	collector
2	base
3	emitter



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	40	V
V_{EBO}	emitter-base voltage	open collector	–	6	V
I_C	collector current (DC)		–	200	mA
I_{CM}	peak collector current		–	300	mA
I_{BM}	peak base current		–	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$; note 1	–	500	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Note

1. Transistor mounted on an FR4 printed-circuit board.

NPN switching transistor

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	250	K/W

Note

1. Transistor mounted on an FR4 printed-circuit board.

CHARACTERISTICS

 $T_{amb} = 25\text{ }^{\circ}\text{C}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0$; $V_{CB} = 30\text{ V}$	–	50	nA
I_{EBO}	emitter cut-off current	$I_C = 0$; $V_{EB} = 6\text{ V}$	–	50	nA
h_{FE}	DC current gain	$V_{CE} = 1\text{ V}$; note 1 $I_C = 0.1\text{ mA}$ $I_C = 1\text{ mA}$ $I_C = 10\text{ mA}$ $I_C = 50\text{ mA}$ $I_C = 100\text{ mA}$	60 80 100 60 30	– – 300 – –	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 1\text{ mA}$; note 1 $I_C = 50\text{ mA}$; $I_B = 5\text{ mA}$; note 1	– –	200 200	mV mV
V_{BEsat}	base-emitter saturation voltage	$I_C = 10\text{ mA}$; $I_B = 1\text{ mA}$; note 1 $I_C = 50\text{ mA}$; $I_B = 5\text{ mA}$; note 1	– –	850 950	mV mV
C_c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = 5\text{ V}$; $f = 1\text{ MHz}$	–	4	pF
C_e	emitter capacitance	$I_C = i_c = 0$; $V_{EB} = 500\text{ mV}$; $f = 1\text{ MHz}$	–	8	pF
f_T	transition frequency	$I_C = 10\text{ mA}$; $V_{CE} = 20\text{ V}$; $f = 100\text{ MHz}$	300	–	MHz
F	noise figure	$I_C = 100\text{ }\mu\text{A}$; $V_{CE} = 5\text{ V}$; $R_S = 1\text{ k}\Omega$; $f = 10\text{ Hz}$ to 15.7 kHz	–	5	dB

Switching times (between 10% and 90% levels); see Fig.2

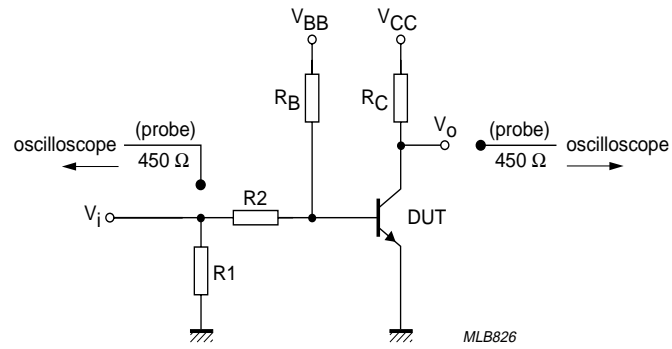
t_{on}	turn-on time	$I_{Con} = 10\text{ mA}$; $I_{Bon} = 1\text{ mA}$; $I_{Boff} = -1\text{ mA}$	–	65	ns
t_d	delay time		–	35	ns
t_r	rise time		–	35	ns
t_{off}	turn-off time		–	240	ns
t_s	storage time		–	200	ns
t_f	fall time		–	50	ns

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

NPN switching transistor

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$V_i = 5 \text{ V}$; $T = 500 \mu\text{s}$; $t_p = 10 \mu\text{s}$; $t_r = t_f \leq 3 \text{ ns}$.
 $R_1 = 56 \Omega$; $R_2 = 2.5 \text{ k}\Omega$; $R_B = 3.9 \text{ k}\Omega$; $R_C = 270 \Omega$.
 $V_{BB} = -1.9 \text{ V}$; $V_{CC} = 3 \text{ V}$.
 Oscilloscope input impedance $Z_i = 50 \Omega$.

Fig.2 Test circuit for switching times.

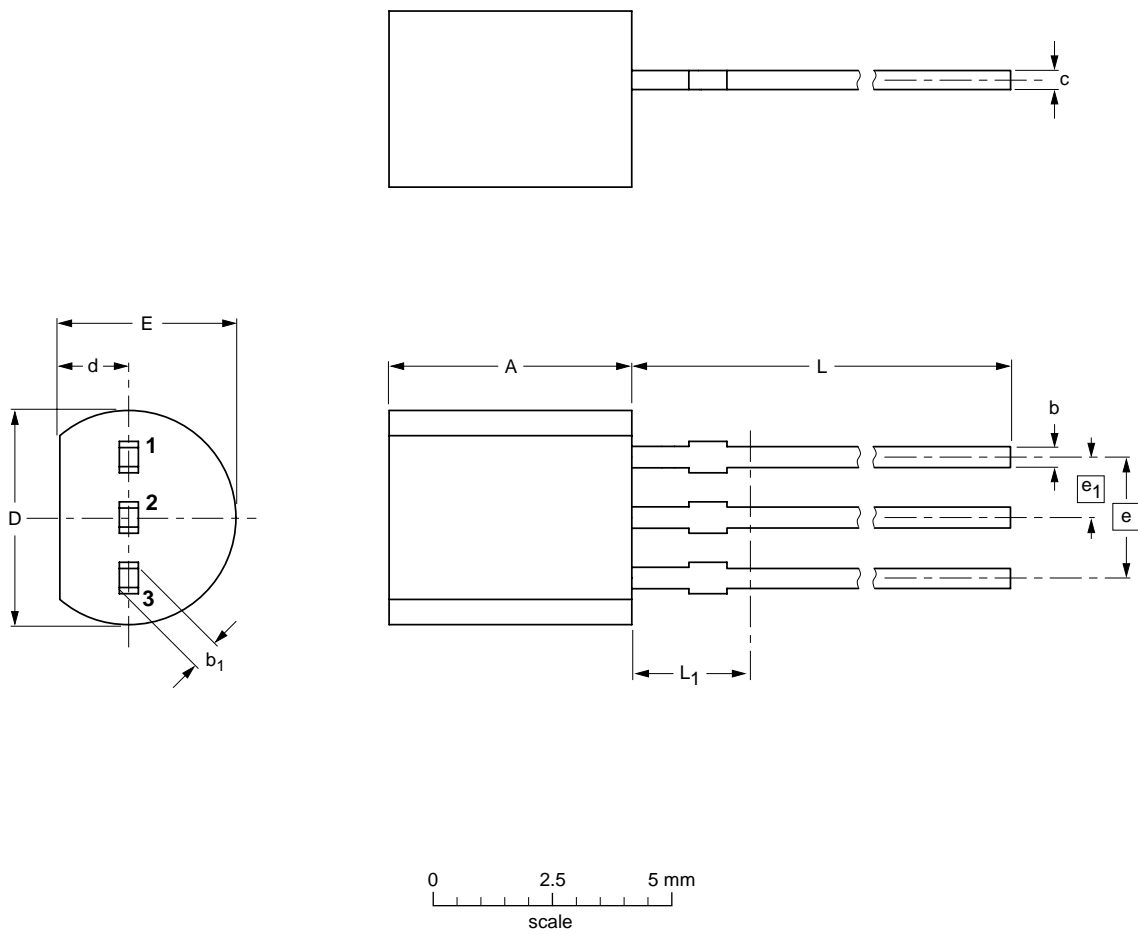
NPN switching transistor

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PACKAGE OUTLINE

Plastic single-ended leaded (through hole) package; 3 leads

SOT54



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b ₁	c	D	d	E	e	e ₁	L	L ₁ ⁽¹⁾
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT54		TO-92	SC-43		97-02-28

NPN switching transistor

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NPN switching transistor

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