Features

- **Number of Keys:**
  - **One**
- **Technology:**
  - **Patented spread-spectrum charge-transfer**
- **Key outline sizes:**
  - **6 mm x 6 mm or larger (panel thickness dependent); widely different sizes and shapes possible**
- **Electrode design:**
  - **Solid or ring electrode shapes**
- **PCB Layers required:**
  - **One**
- **Electrode materials:**
  - **Etched copper, silver, carbon, Indium Tin Oxide (ITO)**
- **Electrode substrates:**
  - **PCB, FPCB, plastic films, glass**
- **Panel materials:**
  - **Plastic, glass, composites, painted surfaces (low particle density metallic paints possible)**
- **Panel thickness:**
  - **Up to 50 mm glass, 20 mm plastic (electrode size and Cs dependent)**
- **Key sensitivity:**
  - **Settable via capacitor (Cs)**
- **Interface:**
  - **Digital output, active high**
- **Moisture tolerance:**
  - **Good**
- **Power:**
  - **2V – 5.5V; 6.5 µA at 2.0V typical**
- **Package:**
  - **6-pin WSON RoHS compliant**
  - **10-pin MSOP RoHS compliant** (available to special order with 50K MOQ)
- **Signal processing:**
  - **Self-calibration, auto drift compensation, noise filtering**
- **Applications:**
  - **Control panels, consumer appliances, toys, lighting controls, mechanical switch or button**
- **Patents:**
  - **QTouch™ (patented charge-transfer method)**

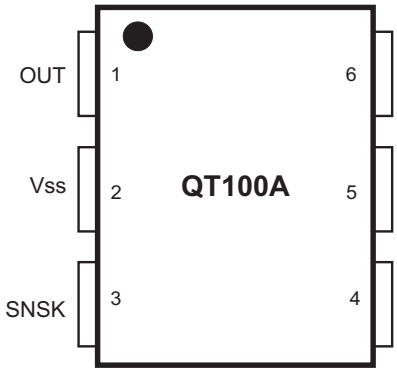
QTouch™ Charge Transfer IC

AT42QT100A

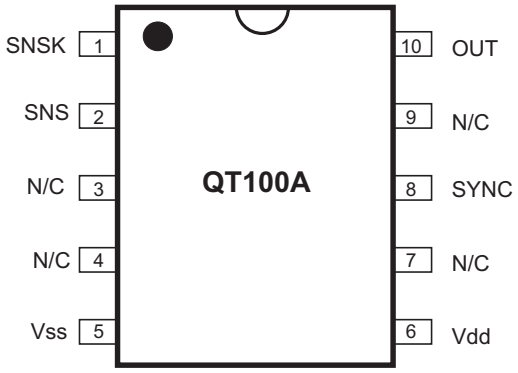
9531A–AT42–02/09

1. Pinout and Schematic

1.1 Pinout Configuration



6-WSON Package



10-MSOP Package

1.2 Pin Descriptions

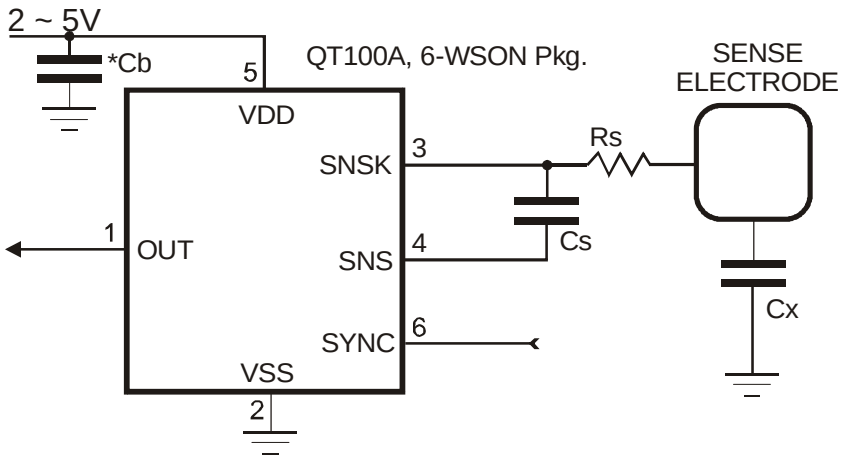
Table 1-1. Pin Listing

Name	6-Pin WSON	10-Pin MSOP	Type	Comments	Notes
SNSK	3	1	I/O	Sense pin	Cs + Key
SNS	4	2	I/O	Sense pin	Cs
N/C	–	3	O	Unused	Leave open – do not connect
N/C	–	4	O	Unused	Leave open – do not connect
Vss	2	5	P	Supply ground	Ground
Vdd	5	6	P	Power	+2.0 ~ +5.0V
N/C	–	7	I	Unused	6-pin package – internally connected to SYNC pin 10-pin package – always connect pin to Sync
SYNC	6	8	I	Sync and Mode Input	6-pin package – pin is either Sync/Slow/Fast Mode, depending on logic level applied (see Section 3.1 on page 5)
N/C	–	9	O	Unused	Leave open – do not connect
OUT	1	10	O	Output state	–

I Input only
I/O Input and output
O Output only, push-pull
P Ground or power

1.3 Schematic

Figure 1-1. Basic Circuit Configuration for 6-pin WSON Package



*Note: Bypass capacitor Cb should be tightly wired between Vdd and Vss

2. Overview of the QT100A

2.1 Introduction

The QT100A charge-transfer (QT™) touch sensor is a self-contained digital IC capable of detecting near-proximity or touch. It will project a touch or proximity field through any dielectric like glass, plastic, stone, ceramic, and even most kinds of wood. It can also turn small metal-bearing objects into intrinsic sensors, making them responsive to proximity or touch. This capability, coupled with its ability to self-calibrate, can lead to entirely new product concepts.

The QT100A is designed specifically for human interfaces, like control panels, appliances, toys, lighting controls, or anywhere a mechanical switch or button may be found. It includes all hardware and signal processing functions necessary to provide stable sensing under a wide variety of changing conditions. Only a single low cost, noncritical capacitor is required for operation.

The QT100A can also project a proximity field to several centimeters with the proper electrode and circuit design.

Two package types are offered, one of which can directly replace the QT100's SOT-23-6 package but with a reduced thickness.

These devices are intended to replace the QT100.

Refer to the following application note for more information on migrating from QT100:

- QTAN0028 – *Sensitivity Differences When Migrating from QT100 to QT100A*

2.1.1 WSON Package Differences with QT100

A 6-pin WSON package version is available which uses the same basic PCB footprint as the QT100's SOT-23-6 package. The 6-WSON package has a reduced package thickness.

In converting an existing design from the QT100 to the QT100A, it should be noted that the 6-WSON package has a bottom "center pad" which must be either grounded (connected to Vss) or isolated. This center pad is wide enough that it can possibly touch the copper pads of the QT100's SOT-23-6 footprint, potentially creating a short circuit between two or more pads. In order to prevent this, the solder mask layer of the PCB should be widened slightly, or, the copper PCB pads narrowed slightly in size.

Refer to the following application note for assistance with this conversion process:

- QTAN0027 – *PCB Design Considerations when Changing from 6-pin SOT23 to 6-pin WSON Atmel® Products*

A 10-pin MSOP package version is also available to special order with 50K MOQ.

2.1.2 Electrical Differences With QT100

In order to compensate for the fact that the QT100A silicon is 30 percent more sensitive to capacitive changes than the QT100, the detection threshold has been increased by 30 percent in the QT100A to compensate. The net effect is that the QT100A is behaviorally identical to the QT100 (apart from no recalibration timeout), and no change in the value of Cs is required to achieve the same sensitivity as the QT100.

2.2 Basic Operation

Figure 1-1 on page 3 shows a basic circuit using the 6-pin WSON package.

The QT100A employs bursts of charge-transfer cycles to acquire its signal. Burst mode permits power consumption in the microamp range, dramatically reduces RF emissions, lowers susceptibility to EMI, and yet permits excellent response time. Internally the signals are digitally processed to reject impulse noise, using a "consensus" filter which requires four consecutive confirmations of a detection before the output is activated.

The QT switches and charge measurement hardware functions are all internal to the QT100A.

2.3 Electrode Drive

For optimum noise immunity, the electrode should only be connected to SNSK.

In all cases the rule Cs>>Cx must be observed for proper operation; a typical load capacitance (Cx) ranges from 5-20 pF while Cs is usually about 2-50 nF.

Increasing amounts of Cx destroy gain, therefore it is important to limit the amount of stray capacitance on both SNS terminals. This can be done, for example, by minimizing trace lengths and widths and keeping these traces away from power or ground traces or copper pours.

The traces and any components associated with SNS and SNSK will become touch sensitive and should be treated with caution to limit the touch area to the desired location.

A series resistor, Rs, should be placed in line with SNSK to the electrode to suppress ESD and EMC effects.

2.4 Sensitivity

2.4.1 Introduction

The sensitivity on the QT100A is a function of things like the value of Cs, electrode size and capacitance, electrode shape and orientation, the composition and aspect of the object to be sensed, the thickness and composition of any overlaying panel material, and the degree of ground coupling of both sensor and object.

2.4.2 Increasing Sensitivity

In some cases it may be desirable to increase sensitivity; for example, when using the sensor with very thick panels having a low dielectric constant. Sensitivity can often be increased by using a larger electrode or reducing panel thickness. Increasing electrode size can have diminishing returns, as high values of Cx will reduce sensor gain.

The value of Cs also has a dramatic effect on sensitivity, and this can be increased in value with the trade-off of slower response time and more power. Increasing the electrode's surface area will not substantially increase touch sensitivity if its diameter is already much larger in surface area than the object being detected. Panel material can also be changed to one having a higher dielectric constant, which will better help to propagate the field.

Ground planes around and under the electrode and its SNSK trace will cause high Cx loading and destroy gain. The possible signal-to-noise ratio benefits of ground area are more than negated by the decreased gain from the circuit, and so ground areas around electrodes are discouraged. Metal areas near the electrode will reduce the field strength and increase Cx loading and should be avoided, if possible. Keep ground away from the electrodes and traces.

2.4.3 Decreasing Sensitivity

In some cases the QT100A may be too sensitive. In this case gain can be easily lowered by decreasing Cs.

3. Operation Specifics

3.1 Run Modes

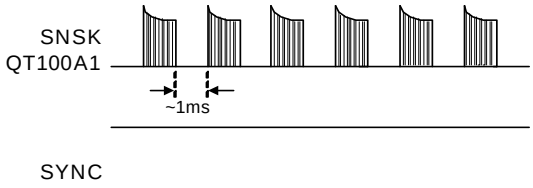
3.1.1 Introduction

The QT100A has three running modes which depend on the logic level applied to the SYNC pin.

3.1.2 Fast Mode (SYNC = 1)

The QT100A runs in Fast mode if the SYNC pin is permanently high. In this mode the QT100A runs at maximum speed at the expense of increased current consumption. Fast mode is useful when speed of response is the prime design requirement. The delay between bursts in Fast mode is approximately 1 ms, as shown in Figure 3-1.

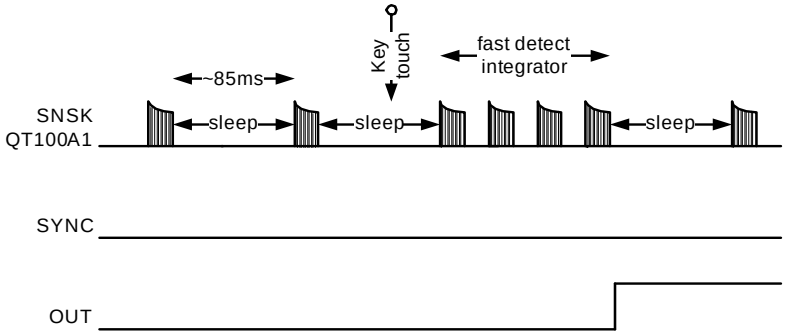
Figure 3-1. Fast Mode Bursts (SYNC Held High)



3.1.3 Low Power Mode (SYNC = 0)

The QT100A runs in Low Power (LP) mode if the SYNC pin is held low. In this mode it sleeps for approximately 85 ms at the end of each burst, saving power but slowing response. On detecting a possible key touch, it temporarily switches to Fast mode until either the key touch is confirmed or found to be spurious (via the detect integration process). It then returns to LP mode after the key touch is resolved, as shown in Figure 3-2.

Figure 3-2. Low Power Mode (SYNC Held Low)

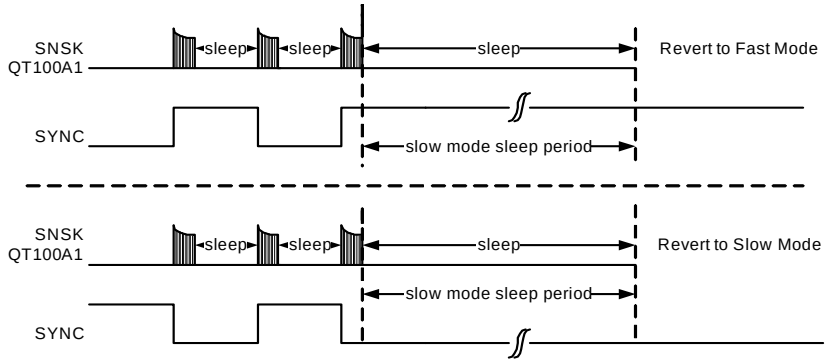


3.1.4 Sync Mode

It is possible to synchronize the device to an external clock source by placing an appropriate waveform on the SYNC pin. Sync mode can synchronize multiple QT100A devices to each other to prevent cross-interference, or it can be used to enhance noise immunity from low frequency sources such as 50Hz or 60Hz mains signals.

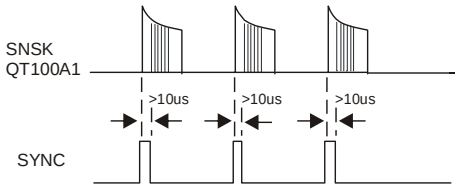
The Sync pin is sampled at the end of each burst. If the device is in Fast mode and the Sync pin is sampled high, then the device continues to operate in Fast mode (Figure 3-1 on page 6). If SYNC is sampled low, then the device goes to sleep. From then on, it will operate in Sync mode (Figure 3-2 on page 6). Therefore, to guarantee entry into Sync mode the low period of the SYNC signal should be longer than the burst length (Figure 3-3).

Figure 3-3. Sync Mode (Triggered by Negative Edges on SYNC)



However, once Sync mode has been entered, if the SYNC signal consists of a series of short pulses (>10 µs) then a burst will only occur on the falling edge of each pulse (Figure 3-4).

Figure 3-4. Sync Mode (Short Pulses)



In Sync mode, the device will sleep after each measurement burst (just as in LP mode) but will be awakened by the falling edge of the SYNC signal, resulting in a new measurement burst. If Sync remains unchanged for a period longer than the LP mode sleep period (about 85 ms), the device will resume operation in either Fast or LP mode depending on the level of the SYNC pin (Figure 3-3).

There is no detect integrator (DI) in Sync mode (each touch is a detection) but the Max On-duration will depend on the time between SYNC pulses; see Section 3.3 on page 7 and Section 3.4 on page 8. Recalibration timeout is a fixed number of measurements so will vary with the SYNC period.

3.2 Threshold

The internal signal threshold level is fixed at 13 counts of change with respect to the internal reference level, which in turn adjusts itself slowly in accordance with the drift compensation mechanism.

The QT100A employs a hysteresis dropout of two counts of the delta between the reference and threshold levels.

3.3 Max On-duration

If an object or material obstructs the sense pad the signal may rise enough to create a detection, preventing further operation. To prevent this, the sensor includes a timer which monitors detections. If a detection exceeds the timer setting the sensor performs a full recalibration. This is known as the Max On-duration feature and is set to ~80s (at 3V). This will vary slightly with Cs and if Sync mode is used. As the internal timebase for Max On-duration is determined by the burst rate, the use of Sync can cause dramatic changes in this parameter depending on the Sync pulse spacing.

3.4 Detect Integrator

It is desirable to suppress detections generated by electrical noise or from quick brushes with an object. To accomplish this, the QT100A incorporates a detect integration (DI) counter that increments with each detection until a limit is reached, after which the output is activated. If no detection is sensed prior to the final count, the counter is reset immediately to zero. In the QT100A, the required count is four. In LP mode the device will switch to Fast mode temporarily in order to resolve the detection more quickly; after a touch is either confirmed or denied the device will revert back to normal LP mode operation automatically.

The DI can also be viewed as a “consensus filter” that requires four successive detections to create an output.

3.5 Forced Sensor Recalibration

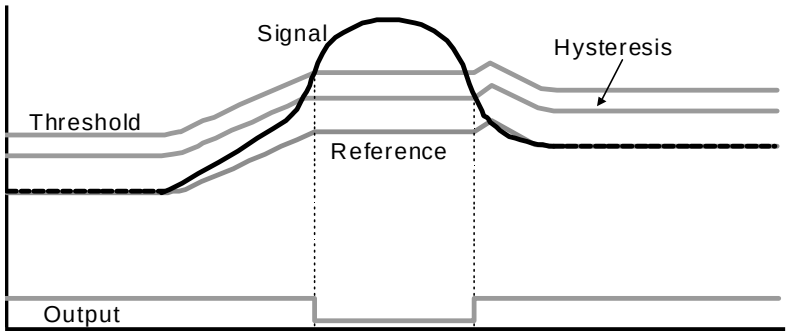
The QT100A has no recalibration pin; a forced recalibration is accomplished when the device is powered up or after the recalibration timeout. However, supply drain is low so it is a simple matter to treat the entire IC as a controllable load; driving the QT100A's Vdd pin directly from another logic gate or a microcontroller port will serve as both power and “forced recalibration”. The source resistance of most CMOS gates and microcontrollers is low enough to provide direct power without problem.

3.6 Drift Compensation

Signal drift can occur because of changes in Cx and Cs over time. It is crucial that drift be compensated for, otherwise false detections, nondetections, and sensitivity shifts will follow.

Drift compensation (Figure 3-5) is performed by making the reference level track the raw signal at a slow rate, but only while there is no detection in effect. The rate of adjustment must be performed slowly, otherwise legitimate detections could be ignored. The QT100A drift compensates using a slew-rate limited change to the reference level; the threshold and hysteresis values are slaved to this reference.

Figure 3-5. Drift Compensation



Once an object is sensed, the drift compensation mechanism ceases since the signal is legitimately high, and therefore should not cause the reference level to change.

The QT100A's drift compensation is asymmetric; the reference level drift-compensates in one direction faster than it does in the other. Specifically, it compensates faster for decreasing signals than for increasing signals. Increasing signals should not be compensated for quickly, since an approaching finger could be compensated for partially or entirely before even approaching the sense electrode. However, an obstruction over the sense pad, for which the sensor has already made full allowance, could suddenly be removed leaving the sensor with an artificially elevated reference level and thus become insensitive to touch. In this latter case, the sensor will compensate for the object's removal very quickly, usually in only a few seconds.

With large values of Cs and small values of Cx, drift compensation will appear to operate more slowly than with the converse. Note that the positive and negative drift compensation rates are different.

3.7 Response Time

The QT100A's response time is highly dependent on run mode and burst length, which in turn is dependent on Cs and Cx. With increasing Cs, response time slows, while increasing levels of Cx reduce response time. The response time will also be a lot slower in LP or Sync mode due to a longer time between burst measurements.

3.8 Spread Spectrum

The QT100A modulates its internal oscillator by ±7.5 percent during the measurement burst. This spreads the generated noise over a wider band reducing emission levels. This also reduces susceptibility since there is no longer a single fundamental burst frequency.

3.9 Output Features

3.9.1 Output

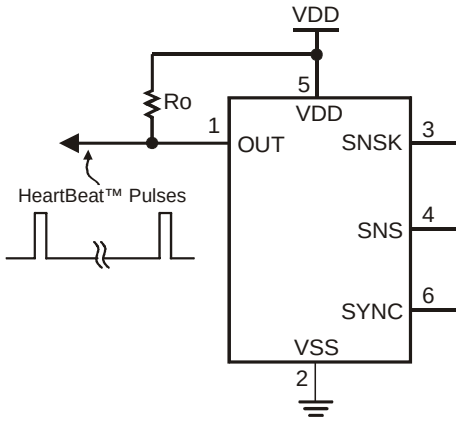
The output of the QT100A is active-high upon detection. The output will remain active-high for the duration of the detection, or until the Max On-duration expires, whichever occurs first. If a Max On-duration timeout occurs first, the sensor performs a full recalibration and the output becomes inactive (low) until the next detection.

3.9.2 HeartBeat™ Output

The QT100A output has a HeartBeat "health" indicator superimposed on it in both LP and Sync modes. This operates by taking the output pin into a three-state mode for 15 µs, once before every QT burst. This output state can be used to determine that the sensor is operating properly, or it can be ignored, using one of several simple methods.

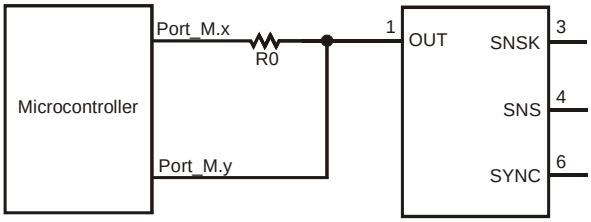
The HeartBeat indicator can be sampled by using a pull-up resistor on the OUT pin (Figure 3-6 on page 10), and feeding the resulting positive-going pulse into a counter, flip flop, one-shot, or other circuit. The pulses will only be visible when the chip is not detecting a touch.

Figure 3-6. Obtaining HeartBeat Pulses with a Pull-up Resistor (6-pin WSON Package)



If the sensor is wired to a microcontroller as shown in Figure 3-7, the microcontroller can reconfigure the load resistor to either Vss or Vdd depending on the output state of the QT100A, so that the pulses are evident in either state.

Figure 3-7. Using a Microcontroller to Obtain HeartBeat Pulses in Either Output State (6-pin WSON Package)



Electromechanical devices like relays will usually ignore the short HeartBeat pulse. The pulse also has too low a duty cycle to visibly affect LEDs. It can be filtered completely if desired, by adding an RC filter to the output, or if interfacing directly and only to a high-impedance CMOS input, by doing nothing or at most adding a small noncritical capacitor from OUT to Vss.

3.9.3 Output Drive

The OUT pin is active high and can sink or source up to 2 mA. When a large value of Cs (>20 nF) is used the OUT current should be limited to <1 mA to prevent gain-shifting side effects, which happen when the load current creates voltage drops on the die and bonding wires; these small shifts can materially influence the signal level to cause detection instability.

4. Circuit Guidelines

4.1 More Information

Refer to Application Note QTAN0002, *Secrets of a Successful QTouch™ Design*, and the *Touch Sensors Design Guide* (both downloadable from the Touch Technology area of Atmel's website) for more information on construction and design methods.

4.2 Sample Capacitor

Cs is the charge sensing sample capacitor. The required Cs value depends on the thickness of the panel and its dielectric constant. Thicker panels require larger values of Cs. Typical values are 2 nF to 50 nF depending on the sensitivity required; larger values of Cs demand higher stability and better dielectric to ensure reliable sensing.

The Cs capacitor should be a stable type, such as X7R ceramic or PPS film. For more consistent sensing from unit to unit, 5 percent tolerance capacitors are recommended. X7R ceramic types can be obtained in 5 percent tolerance at little or no extra cost. In applications where high sensitivity (long burst length) is required the use of PPS capacitors is recommended.

4.3 Power Supply and PCB Layout

See Section 5.2 on page 12 for the power supply range. At 3V current drain averages less than 500 µA in Fast mode.

If the power supply is shared with another electronic system, care should be taken to ensure that the supply is free of digital spikes, sags, and surges which can adversely affect the QT100A. The QT100A will track slow changes in Vdd, but it can be badly affected by rapid voltage fluctuations. It is highly recommended that a separate voltage regulator be used just for the QT100A to isolate it from power supply shifts caused by other components.

If desired, the supply can be regulated using a Low Dropout (LDO) regulator, although such regulators often have poor transient line and load stability. Refer to Application Note QTAN0002, *Secrets of a Successful QTouch™ Design*, and the *Touch Sensors Design Guide* for further information on power supply considerations.

Parts placement: The chip should be placed to minimize the SNSK trace length to reduce low frequency pickup, and to reduce stray Cx which degrades gain. The Cs and Rs resistors (see Figure 1-1 on page 3) should be placed as close to the body of the chip as possible so that the trace between Rs and the SNSK pin is very short, thereby reducing the antenna-like ability of this trace to pick up high frequency signals and feed them directly into the chip. A ground plane can be used under the chip and the associated discrete components, but the trace from the Rs resistor and the electrode should not run near ground, to reduce loading. For best EMC performance the circuit should be made entirely with SMT components.

Electrode trace routing: Keep the electrode trace (and the electrode itself) away from other signal, power, and ground traces including over or next to ground planes. Adjacent switching signals can induce noise onto the sensing signal; any adjacent trace or ground plane next to, or under, the electrode trace will cause an increase in Cx load and desensitize the device. Refer to the *Touch Sensors Design Guide* for further information.

Important Note: for proper operation a 100 nF (0.1 µF) ceramic bypass capacitor must be used directly between Vdd and Vss, to prevent latch-up if there are substantial Vdd transients; for example, during an ESD event. The bypass capacitor should be placed very close to the Vss and Vdd pins.

5. Specifications

5.1 Absolute Maximum Specifications

Operating temperature	-40°C to +85°C
Storage temperature	-55°C to +125°C
V_{DD}	0 to +6.0V
Max continuous pin current, any control or drive pin	±20 mA
Short circuit duration to V_{SS}, any pin	Infinite
Short circuit duration to V_{DD}, any pin	Infinite
Voltage forced onto any pin	-0.6V to (V_{DD} + 0.6) Volts

CAUTION: Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability

5.2 Recommended Operating Conditions

V_{DD}	+2.0 to 5.5V
Short-term supply ripple + noise	±20 mV
Long-term supply stability	±100 mV
Cs value	2 to 50 nF
Cx value	5 to 50 pF

5.3 AC Specifications

V_{DD} = 3.0V, Cs = 10 nF, Cx = 5 pF, Ta = recommended range, unless otherwise noted

Parameter	Description	Min	Typ	Max	Units	Notes
T_{RC}	Recalibration time		250		ms	Cs, Cx dependent
T_{PC}	Charge duration		2		µs	±7.5% spread spectrum variation
T_{PT}	Transfer duration		2		µs	±7.5% spread spectrum variation
T_{G1}	Time between end of burst and start of the next (Fast mode)		1		ms	
T_{G2}	Time between end of burst and start of the next (LP mode)		85		ms	Increases with decreasing V_{DD}
T_{BL}	Burst length		20		ms	V_{DD}, Cs and Cx dependent
T_R	Response time			100	ms	
T_{HB}	HeartBeat pulse width		15		µs	

5.4 Signal Processing

Vdd = 3.0V, Cs = 10 nF, Cx = 5 pF, Ta = recommended range, unless otherwise noted

Description	Min	Typ	Max	Units	Notes
Threshold differential		13		counts	See Note 1
Hysteresis		3		counts	See Note 1
Consensus filter length		4		samples	
Max on-duration		80		seconds	

Note 1: Threshold and hysteresis differ from the QT100 in order to maintain the same sensitivity levels; see Section 2.1.2 on page 4.

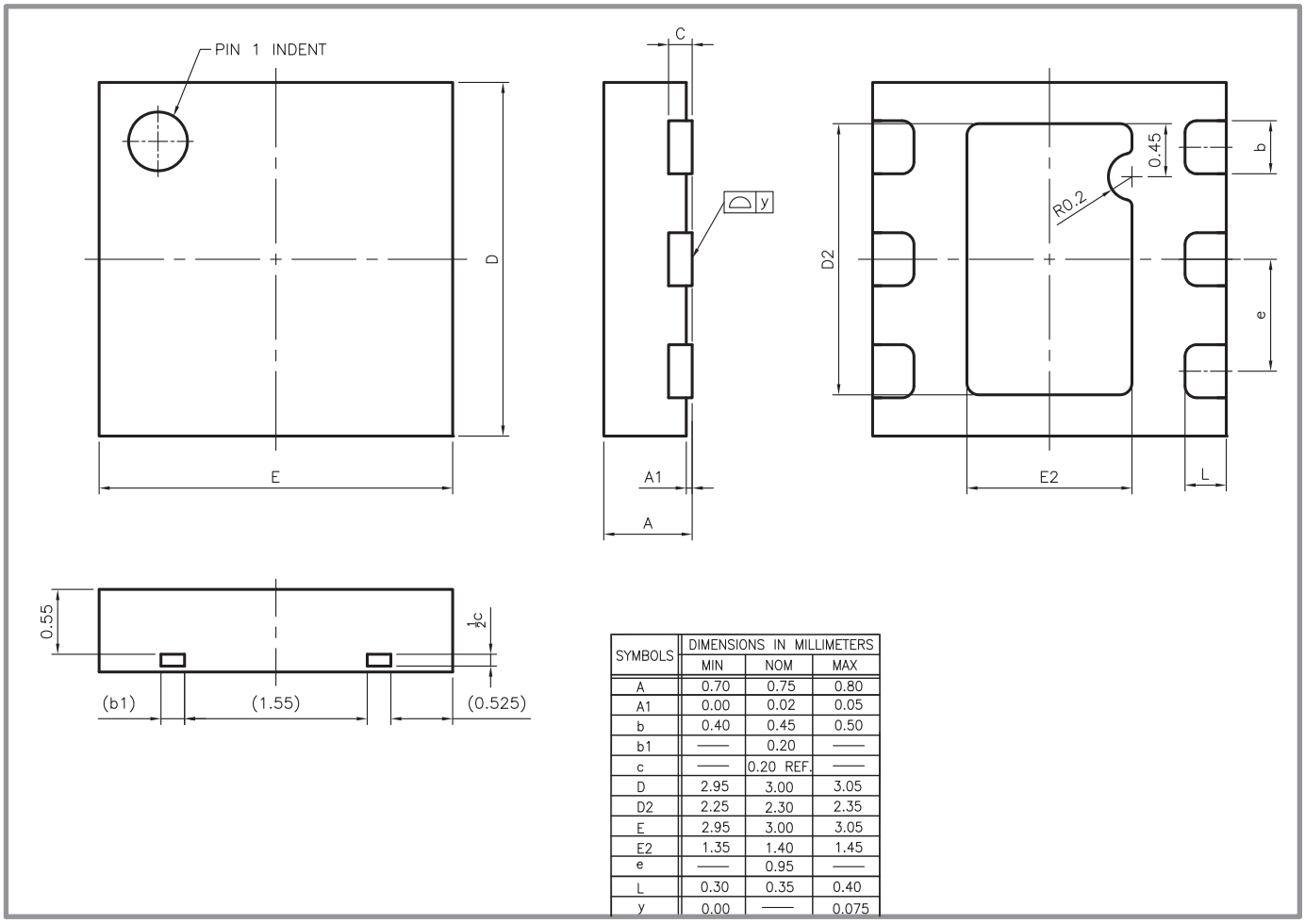
5.5 DC Specifications

Vdd = 3.0V, Cs = 10 nF, Cx = 5 pF, Ta = recommended range, unless otherwise noted

Parameter	Description	Min	Typ	Max	Units	Notes
I_{DD}	Supply current, Fast mode		600		µA	3V
Iddl	Supply current, LP Mode		6.5 17 45	12	µA	2V 3V 5V
V_{DDS}	Supply turn-on slope	100			V/s	Required for proper start-up
V_{IL}	Low input logic level			0.8	V	SYNC pin
V_{HL}	High input logic level	2.2			V	SYNC pin
V_{OL}	Low output voltage			0.6	V	OUT, 4 mA sink
V_{OH}	High output voltage	V_{DD}-0.7			V	OUT, 1 mA source
I_{IL}	Input leakage current			±1	µA	
Cx	Load capacitance range	0		100	pF	
AR	Acquisition resolution		9	14	bits	

5.6 Mechanical Dimensions

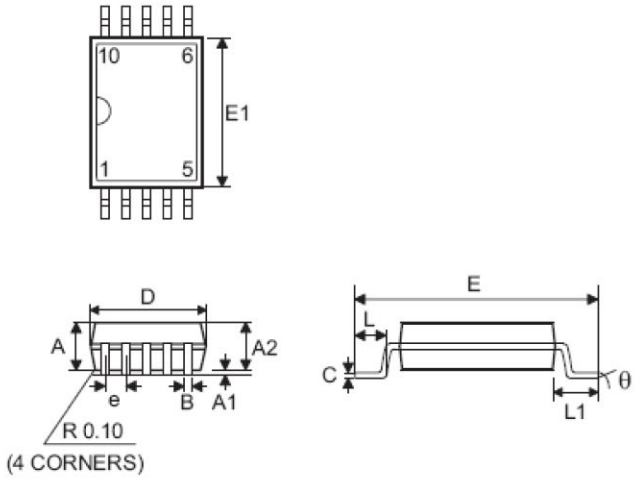
5.6.1 6-pin WSON



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.40	0.45	0.50
b1	——	0.20	——
c	——	0.20 REF.	——
D	2.95	3.00	3.05
D2	2.25	2.30	2.35
E	2.95	3.00	3.05
E2	1.35	1.40	1.45
e	——	0.95	——
L	0.30	0.35	0.40
y	0.00	——	0.075

5.6.2 10-pin MSOP

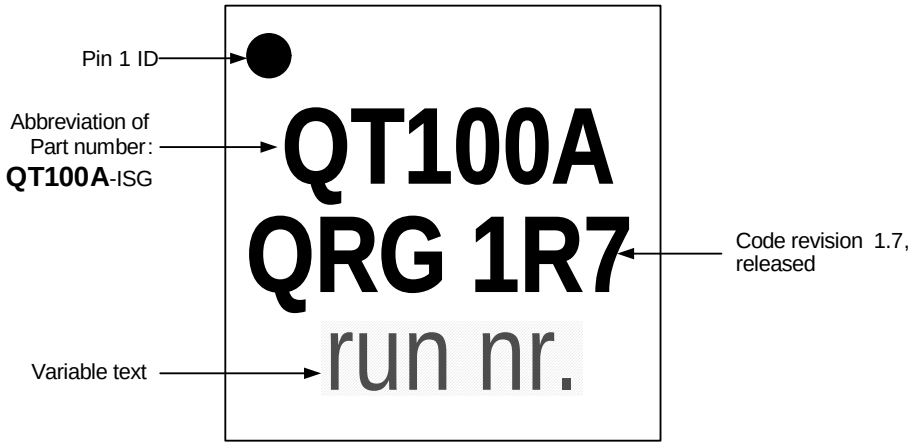
(available to special order with 50K MOQ)



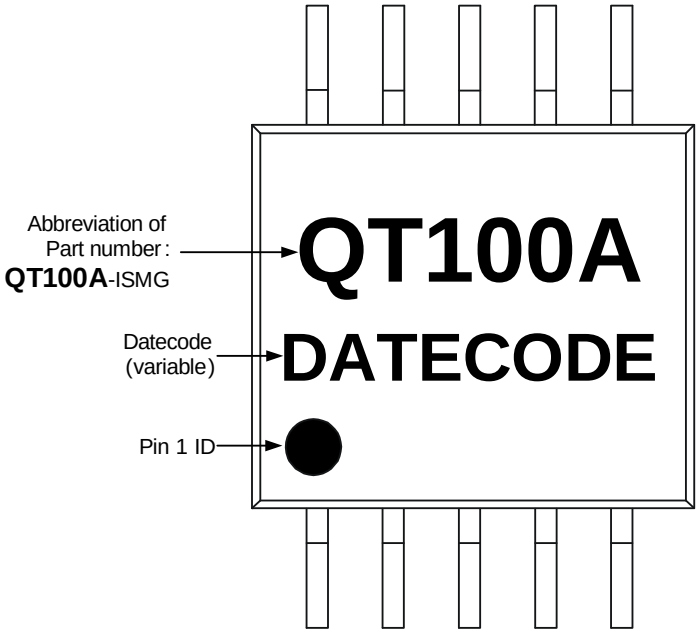
Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	—	1.1
A1	0	—	0.15
A2	0.75	—	0.95
B	0.17	—	0.27
C	—	—	0.25
D	—	3	—
E	—	4.9	—
E1	—	3	—
e	—	0.5	—
L	0.4	—	0.8
L1	—	0.95	—
θ	0°	—	8°

5.7 Marking

5.7.1 6-pin WSON



5.7.2 10-pin MSOP



5.8 Part Number

Part Number	Description
QT100A-ISG	6-pin WSON RoHS compliant IC
QT100A-ISMG	10-pin MSOP RoHS compliant IC (available to special order with 50K MOQ)

5.9 Moisture Sensitivity Level (MSL)

MSL Rating	Peak Body Temperature	Specifications
MSL3	260°C	IPC/JEDEC J-STD-020

Revision History

Revision No.	History
Revision A – February 2009	• Initial release for chip revision 1.7.

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