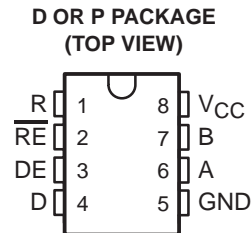


# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

- Bidirectional Transceiver
- Meets or Exceeds the Requirements of ANSI Standards EIA/TIA-422-B and ITU Recommendation V.11
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . .  $\pm 60$  mA Max
- Thermal-Shutdown Protection
- Driver Positive- and Negative-Current Limiting
- Receiver Input Impedance . . . 12 k $\Omega$  Min
- Receiver Input Sensitivity . . .  $\pm 200$  mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates From Single 5-V Supply
- Low Power Requirements



## description

The SN75176A differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. It is designed for balanced transmission lines and meets ANSI Standard EIA/TIA-422-B and ITU Recommendation V.11.

The SN75176A combines a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or  $V_{CC} = 0$ . These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 mA of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 k $\Omega$ , an input sensitivity of  $\pm 200$  mV, and a typical input hysteresis of 50 mV.

The SN75176A can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

The SN75176A is characterized for operation from 0°C to 70°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1995, Texas Instruments Incorporated

# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

## Function Tables

### DRIVER

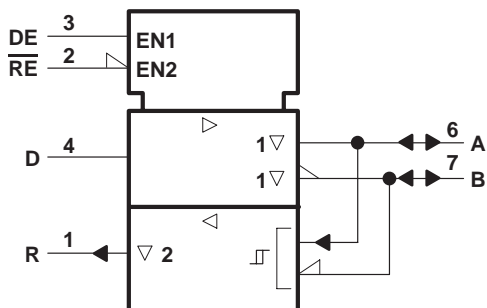
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

### RECEIVER

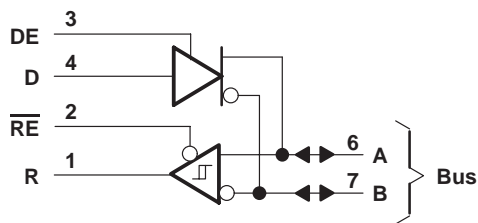
DIFFERENTIAL INPUTS A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2 V$	L	H
$-0.2 V < V_{ID} < 0.2 V$	L	?
$V_{ID} \leq -0.2 V$	L	L
X	H	Z
Open	L	?

H = high level, L = low level, ? = indeterminate,  
X = irrelevant, Z = high impedance (off)

### logic symbol†

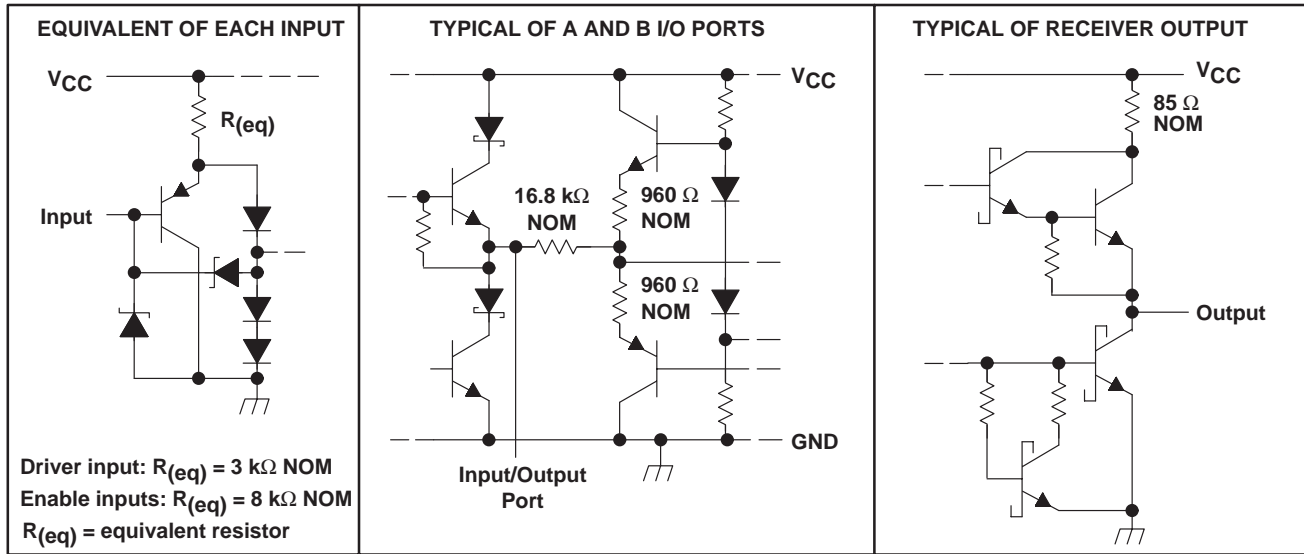


### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**schematics of inputs and outputs**



**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Voltage range at any bus terminal	-10 V to 15 V
Enable input voltage, $V_I$	5.5 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 105^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	261 mW
P	1100 mW	8.8 mW/°C	704 mW	396 mW

# SN75176A

## DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

### recommended operating conditions

		MIN	TYP	MAX	UNIT
Supply voltage, $V_{CC}$		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), $V_I$ or $V_{IC}$		-7		12	V
High-level input voltage, $V_{IH}$	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, $V_{IL}$	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, $V_{ID}$ (see Note 2)				$\pm 12$	V
High-level output current, $I_{OH}$	Driver			-60	mA
	Receiver			-400	$\mu$ A
Low-level output current, $I_{OL}$	Driver			60	mA
	Receiver			8	
Operating free-air temperature, $T_A$		0		70	$^{\circ}$ C

NOTE 2: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



### DRIVER SECTION

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -18$ mA			-1.5	V
$V_{OH}$	High-level output voltage	$V_{IH} = 2$ V, $I_{OH} = -33$ mA $V_{IL} = 0.8$ V,		3.7		V
$V_{OL}$	Low-level output voltage	$V_{IH} = 2$ V, $I_{OH} = 33$ mA $V_{IL} = 0.8$ V,		1.1		V
$ V_{OD1} $	Differential output voltage	$I_O = 0$			$2V_{OD2}$	V
$ V_{OD2} $	Differential output voltage	$R_L = 100$ $\Omega$ , See Figure 1	2	2.7		V
		$R_L = 54$ $\Omega$ , See Figure 1	1.5	2.4		
$\Delta V_{OD} $	Change in magnitude of differential output voltage‡				$\pm 0.2$	V
$V_{OC}$	Common-mode output voltage§	$R_L = 54$ $\Omega$ or $100$ $\Omega$ , See Figure 1			3	V
$\Delta V_{OC} $	Change in magnitude of common-mode output voltage‡				$\pm 0.2$	V
$I_O$	Output current	Output disabled, See Note 3	$V_O = 12$ V		1	mA
			$V_O = -7$ V		-0.8	
$I_{IH}$	High-level input current	$V_I = 2.4$ V			20	$\mu$ A
$I_{IL}$	Low-level input current	$V_I = 0.4$ V			-400	$\mu$ A
$I_{OS}$	Short-circuit output current	$V_O = -7$ V			-250	mA
		$V_O = V_{CC}$			250	
		$V_O = 12$ V			500	
$I_{CC}$	Supply current (total package)	No load	Outputs enabled	35	50	mA
			Outputs disabled	26	40	

† All typical values are at  $V_{CC} = 5$  V and  $T_A = 25^\circ\text{C}$ .

‡  $\Delta|V_{OD}|$  and  $\Delta|V_{OC}|$  are the changes in magnitude of  $V_{OD}$  and  $V_{OC}$  respectively, that occur when the input is changed from a high level to a low level.

§ In ANSI Standard EIA/TIA-422-B,  $V_{OC}$ , which is the average of the two output voltages with respect to GND, is called output offset voltage,  $V_{OS}$ .

NOTE 3: This applies for both power on and off; refer to ANSI Standard EIA/TIA-422-B for exact conditions.

### switching characteristics, $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	$R_L = 60$ $\Omega$ , See Figure 3		40	60	ns
$t_{t(OD)}$	Differential-output transition time			65	95	
$t_{PZH}$	Output enable time to high level	$R_L = 110$ $\Omega$ , See Figure 4		55	90	ns
$t_{PZL}$	Output enable time to low level	$R_L = 110$ $\Omega$ , See Figure 5		30	50	ns
$t_{PHZ}$	Output disable time from high level	$R_L = 110$ $\Omega$ , See Figure 4		85	130	ns
$t_{PLZ}$	Output disable time from low level	$R_L = 110$ $\Omega$ , See Figure 5		20	40	ns

# SN75176A

## DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

### RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>O</sub> = 2.7 V,	I <sub>O</sub> = -0.4 mA			0.2	V	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>O</sub> = 0.5 V,	I <sub>O</sub> = 8 mA	-0.2‡			V	
V <sub>hys</sub>	Input hysteresis voltage (V <sub>IT+</sub> - V <sub>IT-</sub> )				50		mV	
V <sub>IK</sub>	Enable clamp voltage	I <sub>I</sub> = -18 mA				-1.5	V	
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV, See Figure 2	I <sub>OH</sub> = -400 μA,		2.7		V	
V <sub>OL</sub>	Low-level output voltage	V <sub>ID</sub> = -200 mV, See Figure 2	I <sub>OL</sub> = 8 mA,			0.45	V	
I <sub>OZ</sub>	High-impedance-state output current	V <sub>O</sub> = 0.4 V to 2.4 V				±20	μA	
I <sub>I</sub>	Line input current	Other input = 0 V, See Note 3	V <sub>I</sub> = 12 V			1	mA	
			V <sub>I</sub> = -7 V			-0.8		
I <sub>IH</sub>	High-level enable input current	V <sub>IH</sub> = 2.7 V				20	μA	
I <sub>IL</sub>	Low-level enable input current	V <sub>IL</sub> = 0.4 V				-100	μA	
r <sub>i</sub>	Input resistance				12		kΩ	
I <sub>OS</sub>	Short-circuit output current					-15	-85	mA
I <sub>CC</sub>	Supply current (total package)	No load	Outputs enabled			35	50	mA
			Outputs disabled			26	40	

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 3: This applies for both power on and power off. Refer to ANSI Standard EIA/TIA-422-B for exact conditions.

### switching characteristics, V<sub>CC</sub> = 5 V, C<sub>L</sub> = 15 pF, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low-to-high-level output	V <sub>ID</sub> = -1.5 V to 1.5 V,	See Figure 6		21	35	ns
t <sub>PHL</sub>	Propagation delay time, high-to-low-level output				23	35	ns
t <sub>PZH</sub>	Output enable time to high level	See Figure 7			10	30	ns
t <sub>PZL</sub>	Output enable time to low level				12	30	ns
t <sub>PHZ</sub>	Output disable time from high level	See Figure 7			20	35	ns
t <sub>PLZ</sub>	Output disable time from low level				17	25	ns



PARAMETER MEASUREMENT INFORMATION

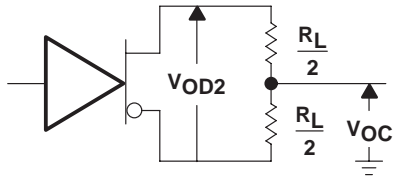


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$

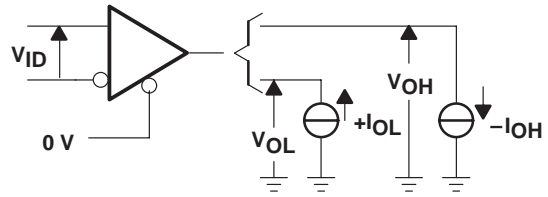
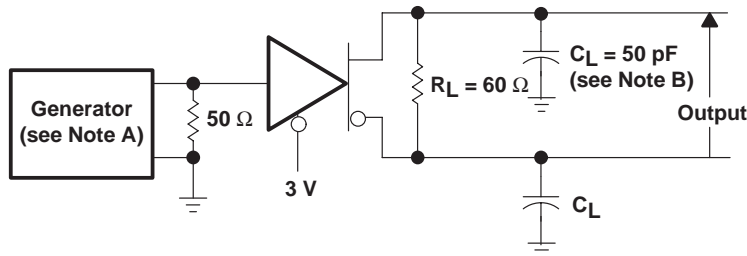
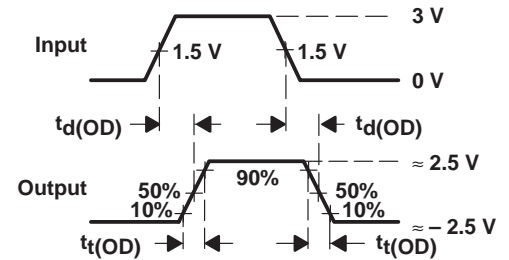


Figure 2. Receiver  $V_{OH}$  and  $V_{OL}$



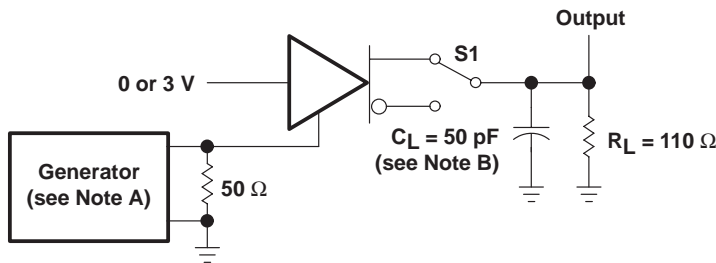
TEST CIRCUIT



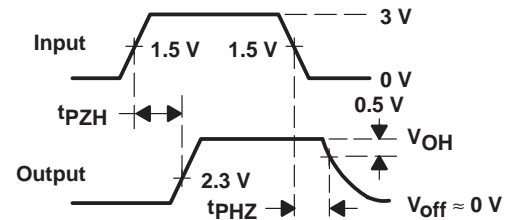
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



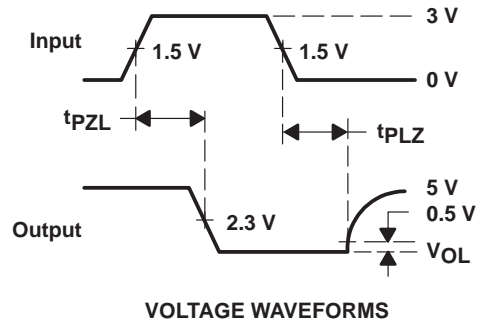
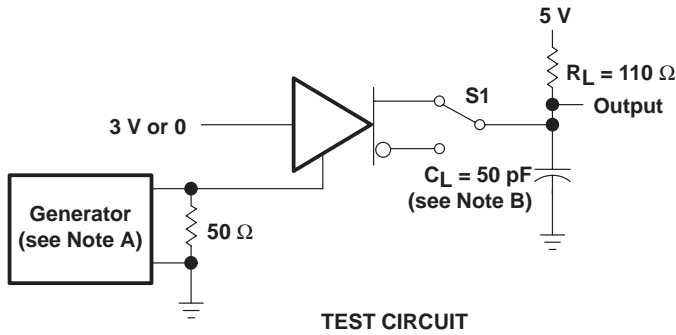
VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

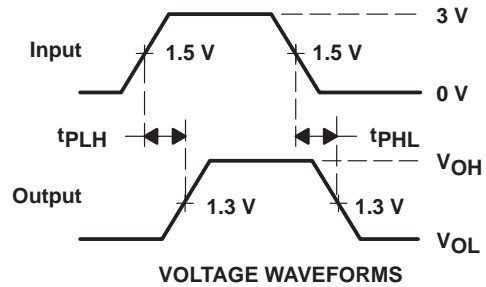
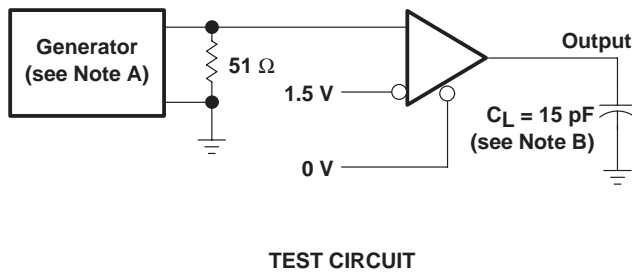
# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995



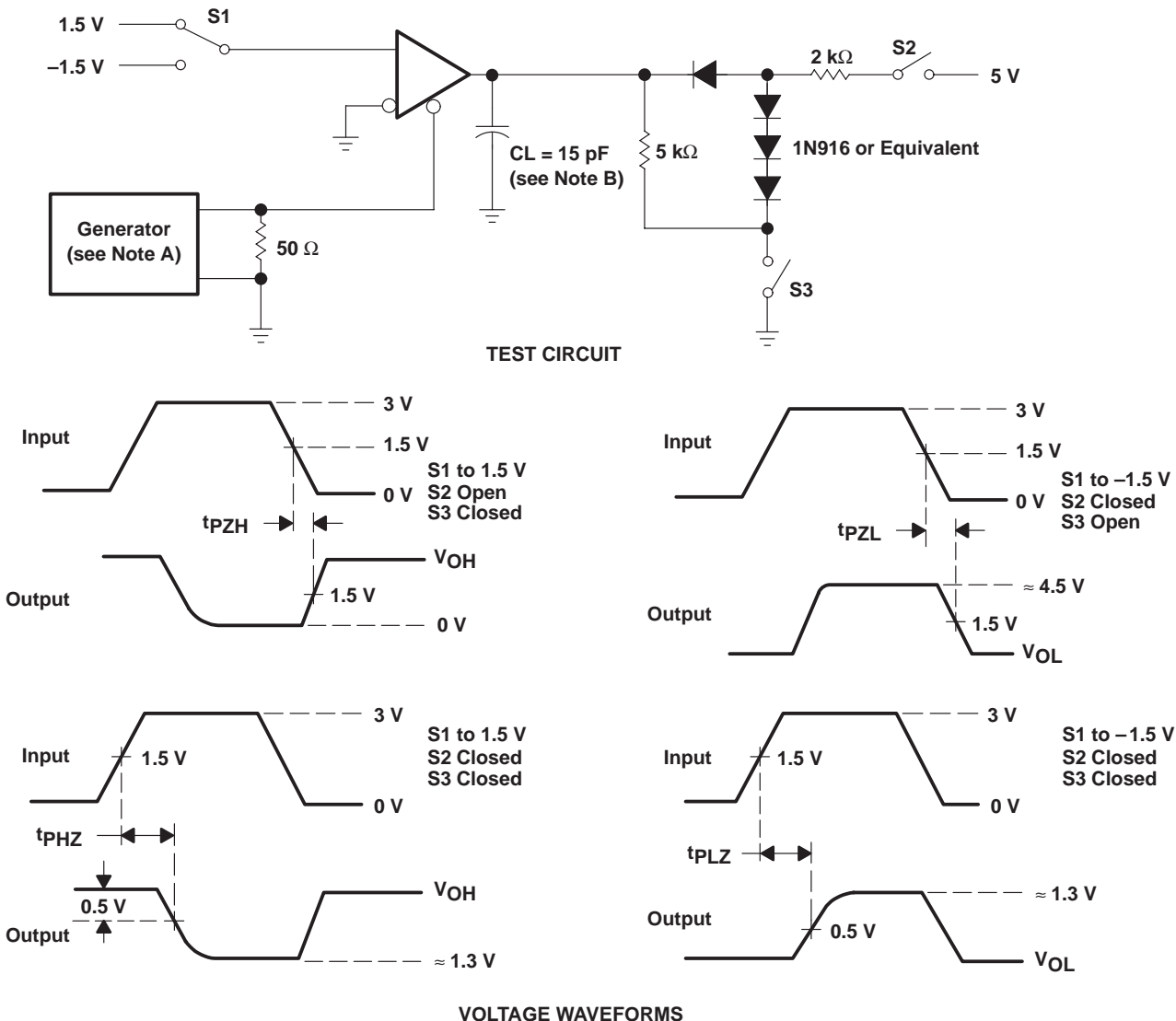
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 5. Driver Test Circuit and Voltage Waveforms**



- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 6. Receiver Test Circuit and Voltage Waveforms**



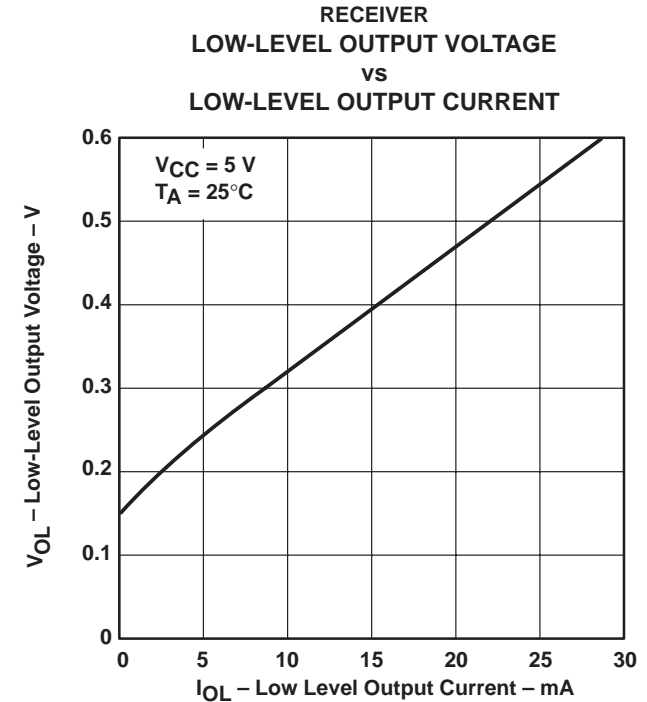
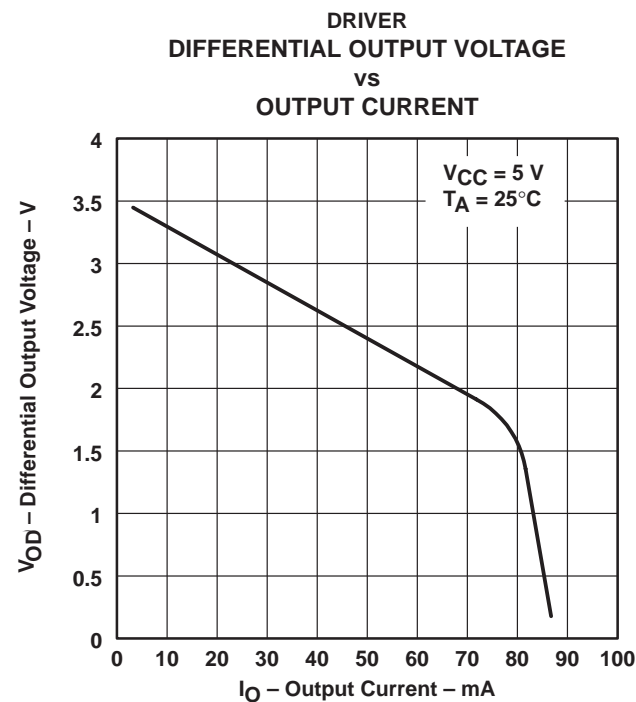
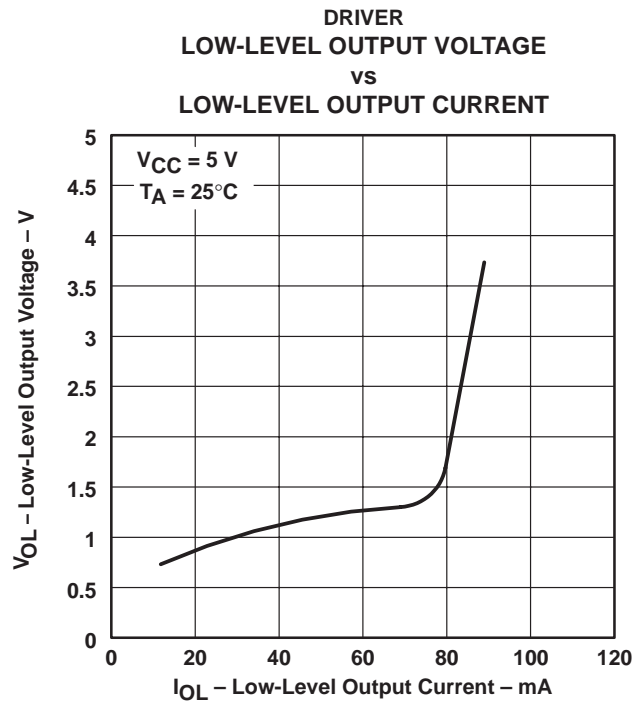
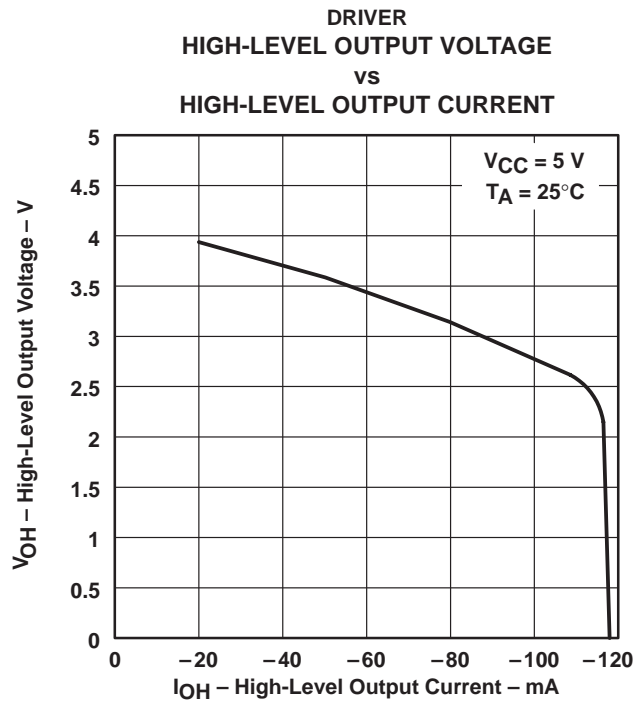
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle,  $t_r \leq 6$  ns,  $t_f \leq 6$  ns,  $Z_O = 50 \Omega$ .  
 B.  $C_L$  includes probe and jig capacitance.

**Figure 7. Receiver Test Circuit and Voltage Waveforms**

# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

## TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

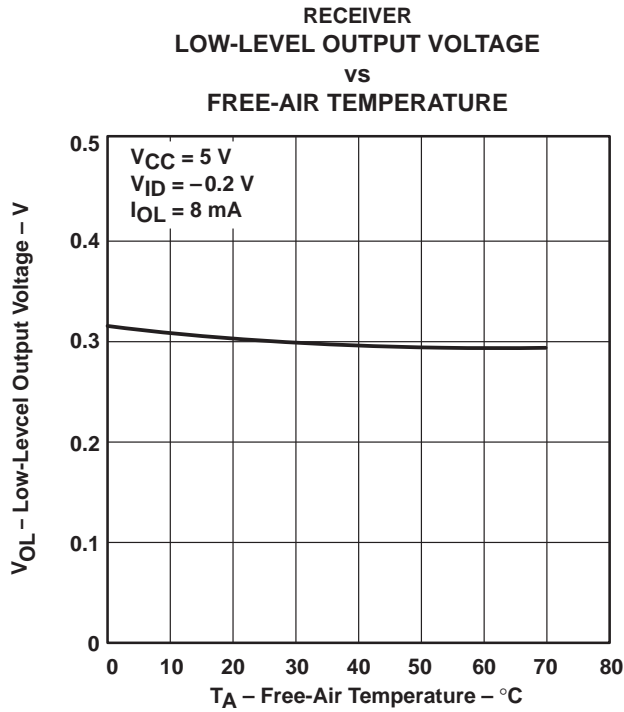


Figure 12

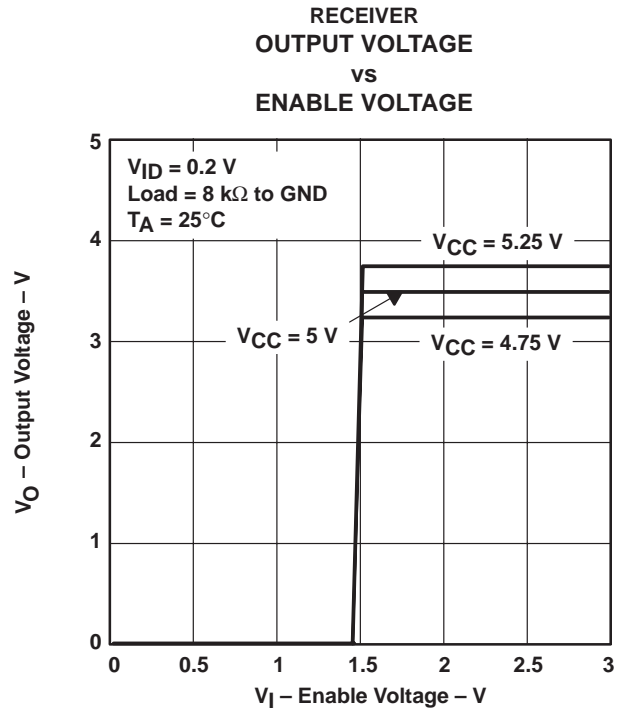


Figure 13

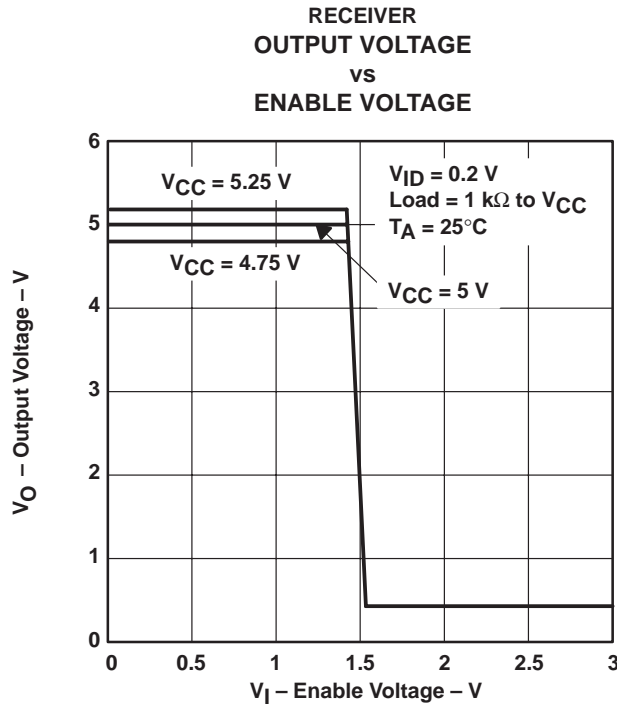
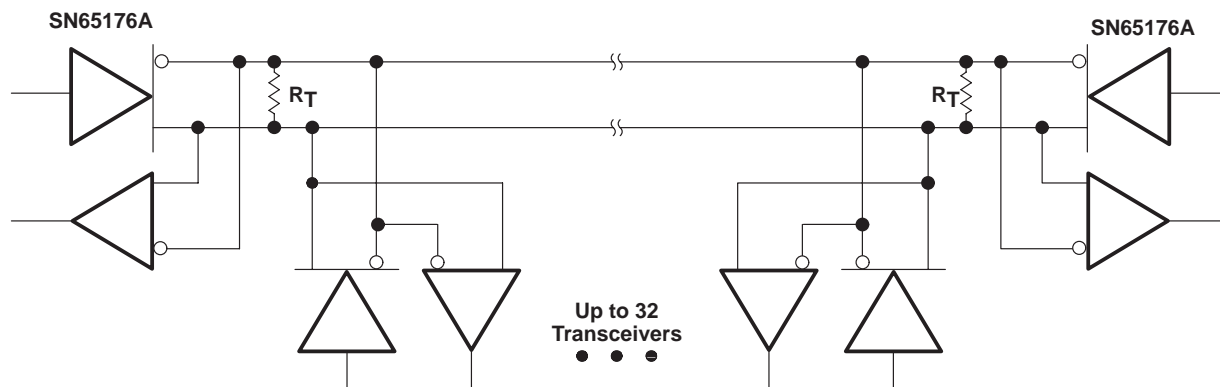


Figure 14

# SN75176A DIFFERENTIAL BUS TRANSCEIVER

SLLS100A – JUNE 1984 – REVISED MAY 1995

## APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ( $R_T = Z_0$ ). Stub lengths off the main line should be kept as short as possible.

Figure 15. Typical Application Circuit

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN75176AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75176AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN75176APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE



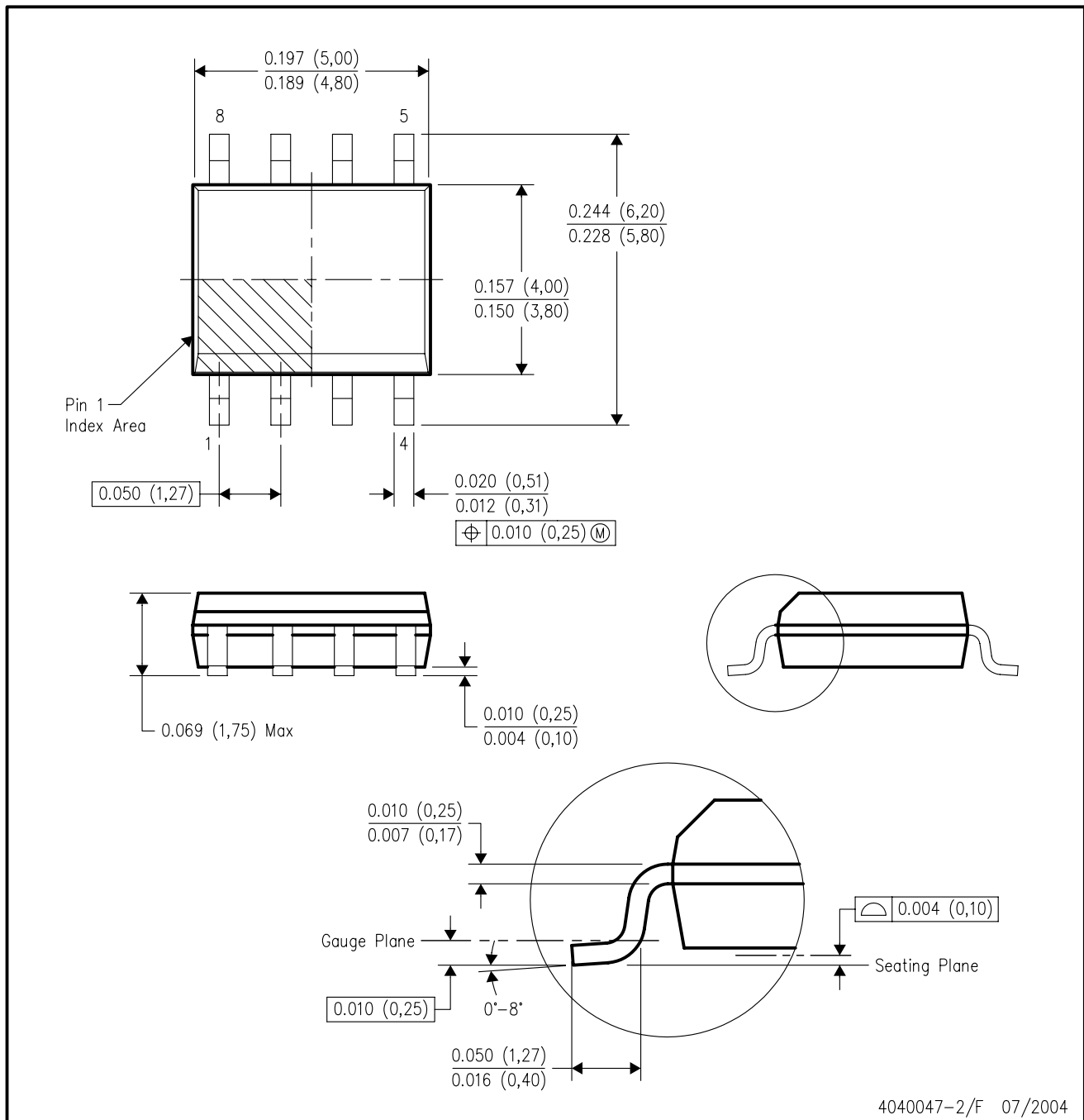
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)



D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2006, Texas Instruments Incorporated